

4/5/2006

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-- DESCRIPTION :  
-- ACTS TO DISTRIBUTE AND ENABLE THE SYSTEM CLOCK TO THE TWO CPLDS. THE CLOCK  
-- LINE IS USED TO INDIVIDUALLY SELECT ONE OR MULTIPLE CPLD'S FOR FUNCTION.  
-- THIS IS DONE BY PROVIDING A CLOCK MASK FROM THE THREE MODULES THAT CONTROL  
-- DAC CONFIGURATION, ADC CONFIGURATION, AND ADC CONVERSION FUNCTIONS.  
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-- IMPLEMENTATION NOTES :  
-- CLOCK MASKS SHOULD ONLY CHANGE WHILE CLK IS HIGH TO PREVENT GLITCHES OR  
-- SHORTENED CLOCK PULSES.  
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```
ADC_ACQ_CLK_MSK : in  std_logic_vector(2 downto 0); -- dlh modified  
CLK              : in  std_logic  
SYSCLK          : out std_logic_vector(2 downto 0); -- dlh modified
```

```
    signal enabl : std_logic_vector(2 downto 0); -- dlh modified
```

```
begin
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```
    enabl(0) <= not (ADC_ACQ_CLK_MSK(0));  
    enabl(1) <= not (ADC_ACQ_CLK_MSK(1));  
    enabl(2) <= not (ADC_ACQ_CLK_MSK(2)); -- dlh
```

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-- The data is synchronous to SYSCLK and travels via pcb traces to the CPLDs so  
-- add a 50% clock delay to the data to eliminate clock <=> data race conditions.  
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```
    SYSCLK(0) <= not CLK or enabl(0);  
    SYSCLK(1) <= not CLK or enabl(1);  
    SYSCLK(2) <= not CLK or enabl(2);    -- dlh
```